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14. ABSTRACT

Si, SiGe, and Ge nanomembrances offer a much more powerful paradigm for the development of silicon optoelectronics overall, not just PCs. Hence explore SiNM fabrication process as a more versatele apporach to Ge-based PCs. Develop membrance processing/ release/transfer - this is a major topic, as there are many parameters that can be modified. Develop membrane stacking procedures - again, these depend on the release and transfer protocols, optimize ways to do this. Characterize Bragg mirrors and simple Si-based PC work with SiNMs. Develop processing ideas for 3D Si-based PCs. Develop contract technology. Develop a theoretical understanding of the relationship of complex index of refraction and charge in SiNMs. Investigate local (from atomic to <100nm) atomic transport, relaxation kinetics, and defect generation at the oxide-Si interface in SOI.

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Photonic Crystals in Silicon via Growth and Preferential Oxidation

Grant # F49620-03-1-0316 1 May 03 to 30 April 07

PI: M. G. Lagally, University of Wisconsin-Madison, Madison, WI 53706
Lagally@engr.wisc.edu

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Photonic crystals consist of engineered arrays of alternating materials with large differences in their refractive indices. In analogy to the electronic behavior of semiconductors, the precise placement and refractive nature of the constituent materials allow the designer to create an optical band gap that prohibits the propagation of a range of light wavelengths. By creating a defect in this ordered structure, such as changing the material spacing in an area, one can create a local region where the previously forbidden light may now propagate.

As most of semiconductor technology rests on silicon, it would be ideal to have photonic crystals produced directly in silicon in a manner compatible with regular Si processing. The ability to do so would facilitate integration of photon manipulators with the electronics needed for their control. One such approach involves patterning photoresist and etching a photonic crystal (PC) into the thin Si template on top of silicon-on-insulator (SOI) to make air gap PCs.

Materials with higher indices of refraction (and larger differences in indices) will reduce the losses inherent in 2D photonic crystals. Larger indices have the added benefit of increasing the photonic bandgap for these devices (see Fig. 1) resulting in an increase in potential bandwidth as more photon energies can be manipulated. A material with higher index of refraction than currently used that is also compatible with

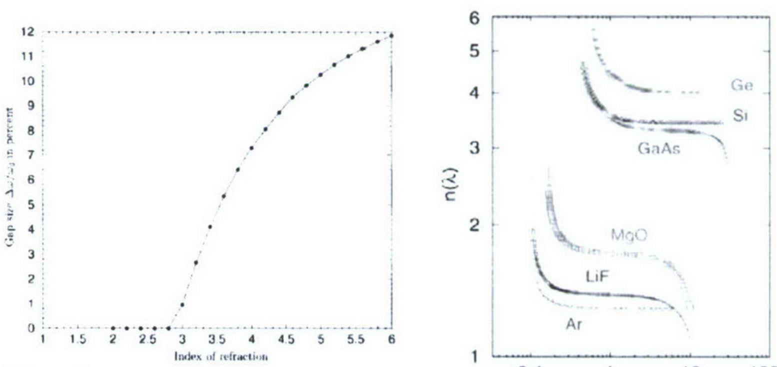

Figure 1

Left: Increase in the photonic bandgap as a function of index of refraction in an air matrix. From Sajeev John and Kurt Busch, IEEE J. Lightwave Tech. 17, 1931 (1999). Right:Wavelength dependence of n. Data from NIST Optical Technology Division

Si is Ge, which has an index of refraction significantly greater than that of either Si or GaAs in the region of interest (4.6 vs. 3.38 and 3.65 at λ=1.55 μm, respectively). Values for SiGe alloys lie between those for Si and Ge.

In this research effort, we are investigating processes to fabricate Si-compatible PCs that have better performance and wider capabilities that those currently being investigated. We have been directing our efforts toward the development and use of free-standing Si nanomembranes (SiNMs) that we have learned to fabricate as the platform for future Si-based PCs. We have asked for a no-cost extension of the grant for one year to allow us to progress this work as much as possible.

The goals of our research are:

- Si, SiGe, and Ge nanomembranes offer a much more powerful paradigm for the development of silicon optoelectronics overall, not just PCs. Hence explore SiNM fabrication process as a more versatile approach to Ge-based PCs
- Develop membrane processing/release/transfer – this is a major topic, as there are many parameters that can be modified
- Develop membrane stacking procedures – again, these depend on the release and transfer protocols, optimize ways to do this.
- Characterize Bragg mirrors and simple SiNM/air PCs to reproduce existing Si-based PC work with SiNMs
- Develop processing ideas for 3D Si-based PCs
- Develop contact technology
- Develop a theoretical understanding of the relationship of complex index of refraction and charge in SiNMs
- Investigate local (from atomic to <100nm) atomic transport, relaxation kinetics, and defect generation at the oxide-Si interface in SOI.

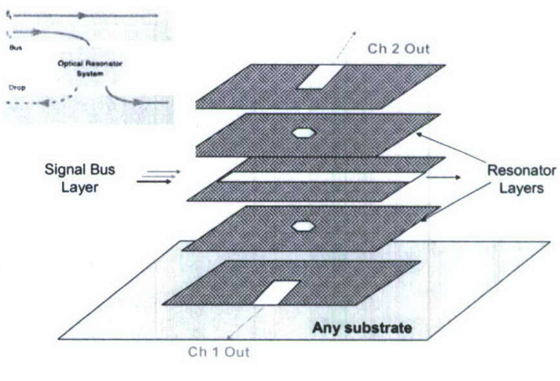

Figure 2. Schematic diagram of a stack of membrane PCs. Each membrane contains a 2D PC made to transmit a particular wavelength. Stacking the membrane layers with resonator layers will produce a device stack that can serve, for example as a channel drop/add filter.

Ultimately we expect to be able to assemble from membranes photonic devices, e.g., add/drop filters, switches, etc., an example of which is schematically shown in Fig. 2. Clearly these goals cannot be accomplished in the remaining time on this grant. We expect to continue this work on future grants.

Progress during the last year

We believe that our approach of using SiNMs offers significant promise for 3D photonic crystals in Si-Ge. The SiNM approach ultimately should let us create novel PCs. Figure 3 shows the membrane fabrication process. The lower right image is an optical micrograph of a completed membrane. The membranes are quite robust. We can use such membranes as individual entities that we can stack. We can build devices into them (CMOS, PCs, Bragg mirrors, etc.) [Local collaborator Jack Ma and students have already fabricated MOSFETs on these membranes, transferred them to flexible hosts and achieved record mobilities and high-frequency performance, *J. Appl. Phys.*, Ref. 4 in the publication list, also *Appl. Phys. Lett.* **89**, 212105 (2006)].

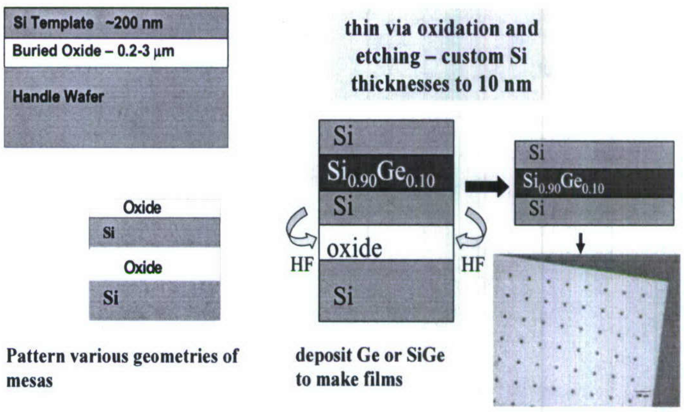

Figure 3. Si nanomembrane fabrication process and image (lower right) of a finished ~200nm elastically strain relaxed multilayer membrane.

Our initial Si nanomembrane investigations focused on the thinning of SOI, the growth, by CVD and MBE, of Si, SiGe, and Ge onto thin SOI, the stability of the initial Si template layer on SOI, the use of strained SOI (sSOI) for growing higher-concentration Ge layers, and the use of SiGe-on-insulator (SGOI). We have also acquired samples of Ge-on-insulator (GOI), via our collaboration with George Celler at Soitec, who has been supplying us with research quality SOI, SGOI, and sSOI free of charge. These investigations have now led to the publications listed below.

We have spent extensive time learning how to pattern these materials at length scales down to the optical and below. We do this with electron beam writing in a LEO 1530 Field Emission SEM, coupled with NGPS electron beam writing software to produce structures with dimensions as little as 20 nm. We have optimized PMMA/MMA deposition with MIBK development and mask-making, at the ~100nm length scale.

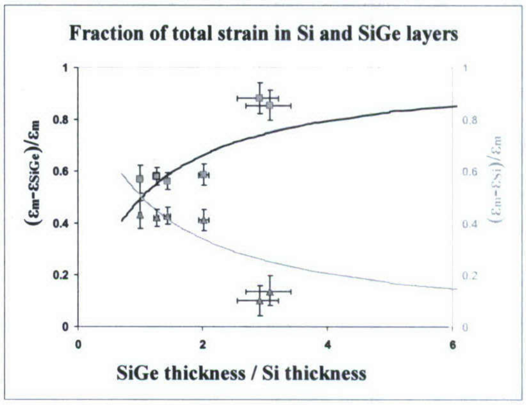

Figure 4. Plot of the fraction of strain transferred to the Si (top curve and data) and fraction of the total strain remaining in the SiGe layers (bottom curve and data) as a function of the ratio of the SiGe total thickness to the Si total thickness assuming perfect elastic strain sharing.

An issue in the transfer process is the possible bending of the very thin membranes during transfer. Transfer processes differ in how much bending may occur. Bending adds additional strain to the strain we introduce by heteroepitaxy. Heteroepitaxy is not necessary to make Si-based multilayered PCs, but the addition of Ge will increase the index of refraction (while also causing strain). Bending can raise the strain to where the membrane structure becomes unstable. Those parameters are important to know. We have made x-ray diffraction measurements and extensive calculations to show what those conditions are for the membranes we typically make. Figure 4 shows calculations and measurements of strain in a membrane. Figure 5 shows calculations of strain as a function of thickness of the central SiGe layer that includes bending strain.

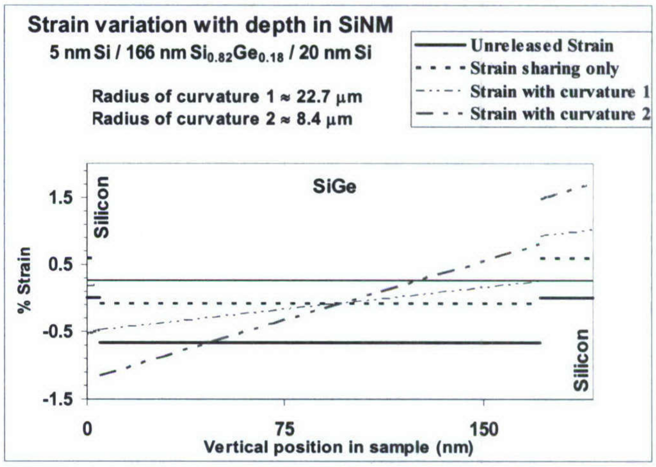

Figure 5. Strain variation as a function of vertical position for the example membrane of 5 nm Si - $Si_{0.82}Ge_{0.18}$ - 20 nm Si for two different radii of curvature. As the curvature decreases, the amount of strain in the top Si layer increases substantially.

In collaboration with Mark Eriksson, we have also made initial studies of stacking of membranes, so far without patterns (other than the access holes for etching that we pattern onto the membrane before release) [W. Peng, et al., *Appl. Phys. Letters*, submitted]. In the stacking of membranes, we first release them into solution and then capture them and place them in a stack. These are Si membranes separated by a spun-on glass, so effectively they are Si/SiO2/Si/SiO_2/... superlattices, with absolutely crystalline Si in each layer. Such superlattices cannot be grown, because the amorphous oxide prevents the epitaxial growth of a single-crystal film. We thus created a Bragg mirror, which in itself is not so novel, as they can be made other ways. But we have demonstrated that one can stack membranes so that they are flat, thin, and defect free. For ultimately fabricating 3D photonic crystals from thin sheets, this capability will be required.

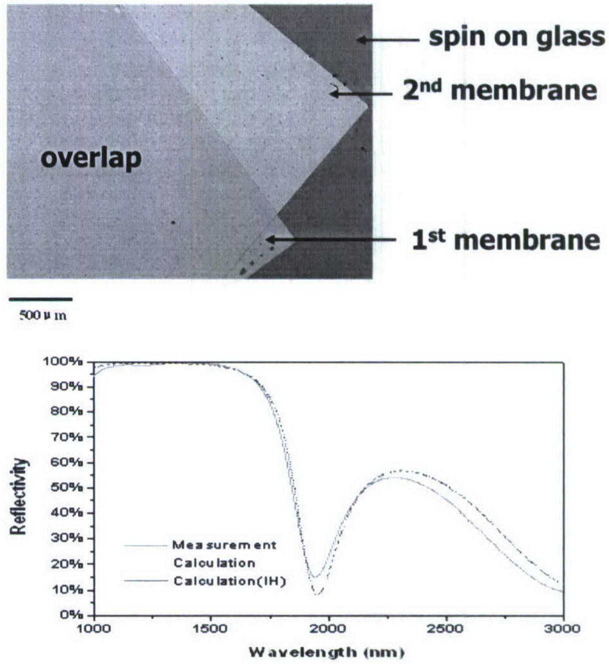

Figure 6. Top: Optical image of two Si membranes separated by a spin-on glass layer. Bottom: IR reflectivity of a 4-membrane stack. The reflectivity is ~100% over a wide range.

Fabrication of electrical contacts to SOI and SGOI substrates, as well as SiNMs continues to be investigated. Issues to be resolved include the effects of interfacial defects formed naturally during the wafer-bonding process and the effects of polycrystalline or amorphous material on the waveguiding capabilities. The inclusion of these additional materials grants more flexibility in the final design of the photonic structures.

We are also continuing to investigate surface transfer doping in nanoscale-dimension Si. The effect should be relevant to nanowires as well, and also to other semiconductors. The problem is that a nano-sized semiconductor may act as an insulator because all dopant charges are trapped by deep trap states. It would thus not be possible to pass any current through them. To put it more succinctly: In bulk semiconductors, a depletion region is formed at the interface of a Schottky contact because of band bending. The depth of the depletion region depends on the material doping, but is typically hundreds of nanometers in high-resistivity material. A similar effect can be created by charge accumulation in surface and interface states, rendering the material partially, or even fully, depleted of free charge carriers. Because the index of refraction is modulated by the density of free carriers, this aspect has repercussions on waveguide design and the potential for all-optical switching. We have made initial investigations of the electronic conductivity in very thin membranes. This is the topic of the *Nature* paper, listed below. Conductivity should be negligible for thin enough membranes, if interface states trap all of the free charge created from dopants. This conclusion turns out to be true if the membrane is bounded by layers that provide deep traps. SiO_2 is such a material. If one of the interfaces presents a band with a density of states close to the "bulk" membrane valence band (as is the case for the surface bands on the (001) Si surface due to the reconstructions, and as we predict for other interfaces), then thermal excitation of carriers from the bulk can cause a very-high-mobility conductivity. We are currently investigating the temperature dependence of this effect to prove it is correct.

We have already shown above that we can produce a 2D photonic crystal in SOI and bulk Si. We therefore will be able to create wavelength specific 2D PCs in membranes. If we stack these, we in principle have a 3D PC. Stacking will require precise alignment, but the methods are similar to nanoimprint lithography in the requirements and specifications.

We are currently working to pattern GOI to make a single-layer 2D photonic crystal using Ge. We will overgrow with oxide to see how a 2D Ge/oxide PC compares in performance with a Si/air gap PC.

Publications, Presentations, and Recognition of the Work

A number of papers have now been published and have attracted considerable attention, with a huge notice by the press. Several new invited papers have been given in the last year, and these have involved discussion of the work supported by this grant. They include the SiRF06 Conference, San Diego Jan 06, the Spring MRS meeting in San Francisco (March 06), the International Conference on Nanoscience and Technology (Basel, July 06), the fall MRS meeting (December 06),.and, upcoming, a plenary lecture at the annual meeting of the DOE Center for Integrated Nanotechnologies (CINT) in Albuquerque, Jan 07. Also we organized a very successful symposium at the APS March meeting, which created sufficient interest so that *Science* wrote a summary of the symposium and a follow-up article. Six invitations to write reviews have been received, and four have now been completed. They are also listed below, as to be published or in press. Publications during the past year that had AFOSR support at least in part include

1. "Electronic Transport in Nanometer-Scale Silicon-on-Insulator", P. P. Zhang, Emma Tevaarwerk, B.-N. Park, D. E. Savage, G. Celler, I. Knezevic, P.G. Evans, M. A. Eriksson, and M. G. Lagally, *Nature* 439, 703 (2006).

2. "Elastically Relaxed Free-Standing Strained-Si Nanomembranes", M.M. Roberts, L.J. Klein, D.E. Savage, M. Friesen, G. K. Celler, M.A. Eriksson, and M.G. Lagally, *Nature Materials* 5, 388 (2006).

3. "Fabrication and Transistor Demonstration on Si-based Nanomembranes", H.-C. Yuan, M. M. Roberts, D. E. Savage, M. G. Lagally, Z. Ma, and G. K. Celler, in *Technical Proceedings of the 2006 Nanotechnology Conference and Trade Show*, Vol. 1, p. 68, NSTI, Danville, CA (2006).

4. "High-Speed Strained-Single-Crystal Silicon Thin-Film Transistors on Flexible Polymers", H.C.Yuan, Z.Q. Ma, M. M. Roberts, D. E. Savage, and M. G. Lagally, *J. Appl. Phys.* 100, 013708 (2006).

5. "Electrical Conductivity in Silicon Nanomembranes", P.P. Zhang, E. P.Nordberg, B.-N. Park, G. K. Celler, I. Knezevic, P.G. Evans, M. A. Eriksson and M. G. Lagally, *New Journal of Physics* 8, 200 (2006).

6. "Scanning Tunnelling Microscopy of Ultra-thin Silicon-on-Insulator", P. P. Zhang, E. Tevaarwerk, B. N. Park, D. E. Savage, G. Celler, I. Knezevic, P. G. Evans, M. A. Eriksson, and M. G. Lagally, *Springer Proceedings in Physics* 110, 341 (2006).

7. "Silicon-Based Nanomembrane Materials: The Ultimate in Strain Engineering", Hao-Chih Yuan, M. M. Roberts, PP Zhang, B.-N. Park, L. J. Klein, D. E. Savage, F.

S. Flack, ZQ Ma, P. G. Evans, M. A. Eriksson, G. K. Celler, and M. G. Lagally, *Digest of Papers, 2006 Topical Meeting on Si Monolithic Integrated Circuits in RF Systems (SiRF06)*, ed. R. Drayton, IEEE, Piscataway, NJ (2006).

8. "Silicon Nanomembranes", M.G. Lagally, MRS Bulletin 32, 57 (2007).

9. "Elastically Strain Sharing Nanomembranes: Flexible and Transferable Strained Silicon and Silicon-Germanium Alloys", S. A. Scott and M. G. Lagally, J. Phys. D. Applied Physics 40, R1 (2007) (invited).

10. "Strained Si-based Nanomembrane Materials", S. A. Scott, M. M. Roberts, D. E. Savage, and M. G. Lagally, MRS Proceedings, submitted

11. "Strain Engineered Silicon Nanomembranes", M.G. Lagally, J. of Physics, Conference Series (JPCS) (invited) in press

Technology Transitions

We continue the quite successful collaboration with George Celler from SOITEC. MGL has written a summary note ["Nanomembranes: Just Around the Bend", Advanced Substrate News, Winter 06-07, http://www.advancedsubstratenews.com] for the online SOITEC newsletter. Celler is a joint author of many of the publications. We have obtained laboratory (noncommercial) samples of GOI from him, as well as all of our SOI and SGOI.

Further collaborations with Walter Buchwald of AFRL Hanscomb are awaiting the development of our ability to make some supporting measurements to what he has done and/or is capable of doing. We has measures some electrical properties of SiNM interfaces for us.

The parallel work on imaging systems has attracted the interest of Micron, Inc. and may lead to a spin-out technology company. A company name. HINODE, Inc., and structure has been chosen, with the PI as one of the founders. Negotiations are underway.

A second technology transfer is in the planning stage, to a new startup called LST Optics, Inc. This company will initially focus on adaptive optics using deformable Si nanomembranes.

International Collaborations

We are attempting to initiate a collaboration with Oliver Schmidt at the Max Planck Institute in Stuttgart, who is active in optoelectronics of Si nanomembranes in the rolled up form. There are some beautiful synergisms that could result. He is presently moving his research group to the University of Dresden, so the start of a collaboration is delayed.